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Multi-layer atom chips for atom tunneling experiments near the chip surface

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ABSTRACT

This paper describes the design and fabrication of an atom chip to be used in ultra-high-vacuum cells for cold-atom tunneling experiments. A fabrication process was developed to pattern micrometer- and nanometer-scale copper wires onto a single chip. The wires, with fabricated widths down to 200 nm, can sustain current densities of more than 7.5×10^7 A/cm^2. Partially suspended wires, developed in order to reduce the Casimir–Polder force between atoms and surface, were also fabricated and tested. Extensive measurements for variable wire width show that the sustainable currents are sufficiently large to allow chip-based atom tunneling experiments. Such chips may allow the realization of an atom transistor.
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1. Introduction

Atom-chip technology [1–9] has been developed rapidly over the last decade as a tool to control ultracold atoms. Micromachined supported and free-standing current-carrying wires on the atom chips have been used to create microscopic magnetic potentials for cooling, trapping, and transport of ultracold atoms. The atom-chip approach enables a variety of methods for manipulating cold atoms and obtaining a Bose–Einstein condensate (BEC) and related forms of ultracold matter. It mitigates the need for high-power, water-cooled magnetic coils and large power supplies. Typically when producing a BEC in a chip-based magnetic trap less than 5 W of power is dissipated by the chip, with current densities up to 10^8 A/cm^2. Under normal conditions this produces a trap with average trap frequencies of more than 1 kHz and a trap depth of more than 1 mK. The tight traps that can be achieved with atom chips allow for fast evaporative cooling of the atoms, which can lead to higher bandwidths for ultracold-atom sensors, and relaxes vacuum requirements.

Atom chips offer the prospect of integrated cold-atom circuits capable of complex functionality. They can be constructed from elementary building blocks as is done in microelectronics, and they may prove useful in fundamental physics research, precision scientific measurements, and quantum information technology [10–15]. A basic component of a conventional electronic circuit is the transistor. Cold-atom transistors have been proposed and theoretically investigated [16,17]. The simplest atom transistor utilizes a three-well potential in which quantum mechanical tunneling between "source" and "drain" wells is controlled by the number of atoms in the central "gate" well as shown in Fig. 1. When the number of atoms in the middle well is small, atom tunneling from the left into the right well is negligible (Fig. 2(a)). This is due to mismatched chemical potential between the middle well and the two other wells (Fig. 2(c)). Adding atoms to the middle well increases the chemical potential due to inter-atomic interactions (Fig. 2(d)) and enables tunneling of atoms from the left to the right well [16]. With appropriate choice of the potential, it is possible to control a large atom flux with a small number of atoms: behavior similar to that of an electronic transistor with current gain.

In order to achieve adequate tunneling rates in the device, the potential minima of the three wells should be as close together as possible; in the order of 1 μm or less. Ideally the sub-micrometer wires used to control atoms are suspended above the chip surface to mitigate the deleterious effects of atom-surface interactions [18]. Incorporating large current-carrying wires on the same substrate as sub-micrometer suspended wires presents a variety of technical challenges. The combination of electron-beam lithography and silicon micromachining techniques enables the fabrication of mechanical structures on the sub-micrometer scale. In this paper, we present a combination of techniques to demonstrate a chip capable of performing two-well atom tunneling experiments, with an eye towards more complicated structures that would enable the realization of an atom transistor. The details of

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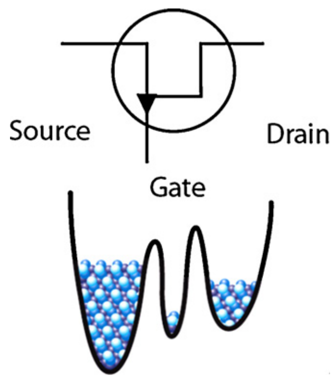

Fig. 1. The schematic drawing of an atom transistor.

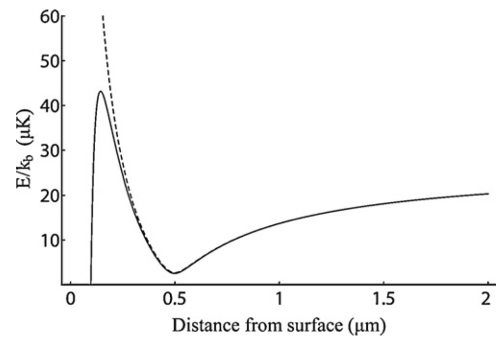

Fig. 3. Plot of the effects of the Casimir–Polder potential on the magnetic trap. Shown are the potentials for the nanowires directly on the surface (solid) and for the wires suspended 2 μm above the surface (dashed).

the design and fabrication process are described in the following sections.

2. Design of the atom transistor chip (theory and simulations)

The intended experiments rely on quantum mechanical tunneling of atoms between adjacent potential energy wells formed by magnetic fields. The potential must be designed to have tunneling rates that are large compared to the inverse lifetime of the atoms, which is about 100 ms when the atoms are within a few hundred nanometers of the chip surface [18], and the tunneling rate should not depend too sensitively on the well depth or atomic energy. The tunneling rate between wells can be estimated using a simple WKB calculation [19], which tells us that to satisfy the above conditions, the traps should be separated by not more than 1 μm. In order for the trap to have features of that scale, the trap has to be formed within the same distance of the wires, and the wire features must be below 1 μm. Unfortunately, fundamental problems arise when the atoms are placed so close to the surface: the attractive Casimir–Polder force between the atoms and the substrate will overpower the potential generated by the chip wires, and the atoms will crash into the surface. To mitigate this effect, we plan to use 100–500 nm wide wires suspended a few micrometers above the chip substrate. The primary loss mechanism of atoms due to the Casmir–Polder attraction will be tunneling of atoms through the magnetic potential into the chip surface. Since both the Casimir potential and the tunneling rate are extremely strong functions of distance a very small relief will be sufficient to make the surface interaction negligible. We estimate that a 2 μm relief should be adequate, which is consistent with the results of Ref. [18]. Fig. 3 shows the potential that the atom experiences for the case of the wire directly on the surface (solid) and when suspended 2 μm above the substrate (dashed). The Casimir–Polder potential is calculated using the method described in Ref. [20]. By placing several of these suspended wires in close proximity, it is possible to form multiple-well potentials with non-negligible tunneling rate (Fig. 4).

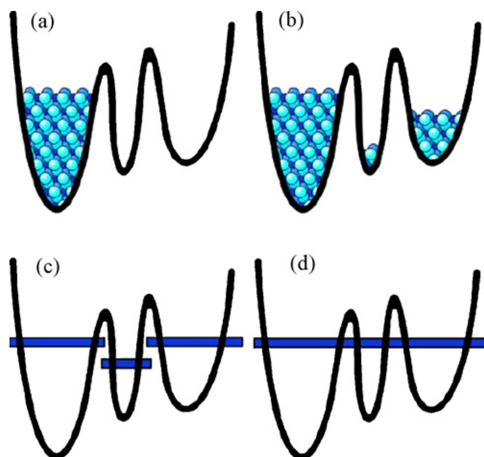

Fig. 2. The atom transistor uses a Bose–Einstein condensate in a triple-well potential.

The nano-bridge wires confine the atoms tightly perpendicular to the direction of the nanowires. To generate a weak confinement in the other direction, we embed three wires into the silicon several micrometers beneath the nano-bridges as shown in Fig. 4(a). The three wires allow the trap to be operated in either the H-trap [21] or the dimple trap [22] configuration.

3. Fabrication of the atom transistor chip

The atom transistor chip (Fig. 5) is created by a multi-layer metallization process with sacrificial oxide layers. The chip is made from a p-type double-side polished, 3 in. diameter silicon wafer (100 cut, 380 μm thick). A 300 nm thick silicon dioxide layer (SiO_2) was grown on both sides of the wafer as an insulating layer. Silicon etch windows on the oxide layer are patterned by HF (48%) for 15 s. A positive photoresist (AZ 4620) was then spin coated on one side of the substrate. After spinning, the wafer was baked on a hotplate for 5 min at 110 °C. After baking, the final thickness of the photoresist is around 6.5 μm. The three silicon trench etch windows (3 μm wide) are then patterned. The lithography is done with a mercury light source with a wavelength of 365 nm. The exposure time is 70 s and the developing time is 2.5 min in a dilute developer (1 part of AZ400K and 3 parts of DI water) at room temperature. The silicon trenches (2 μm deep) were etched by reactive ion etching (RIE). After the RIE etching, the photoresist was kept on the substrate for the self-alignment of the next two process steps: oxide sputtering and copper deposition. In order to have an insulating layer inside the silicon trenches, 100 nm oxide was sputtered inside the trenches. An adhesion layer, chromium (30 nm), and the bottom three copper wires (2 μm) were evaporated to fill up the silicon trenches. After metal evaporation, a lift-off process was performed to remove the metal layer from the surface of the substrate, except for the three embedded copper wires. A sacrificial oxide layer (3 μm) was sputtered on the top of the substrate. After oxide sputtering, the surface of the sputtered oxide was found not to be flat due to the three embedded copper wires underneath. Therefore, a chemical mechanical polishing (CMP) process was utilized to planarize the sputtered oxide surface as shown in Fig. 6(a) and (b). After the planarization, 1 μm of the sputtered oxide was removed. The photoresist used for electron-beam lithog-

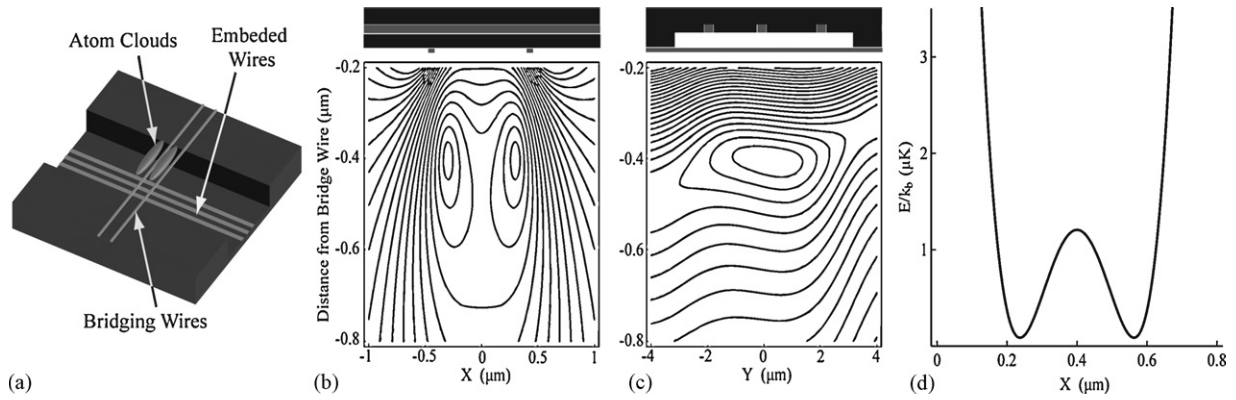

Fig. 4. (a) Schematic diagram of the proposed atom chip. (b) Double well formed perpendicular to the bridging wires. (c) The shape of one trap parallel to the bridging wires. Contour lines indicate equipotential surfaces. Shown above the graphs (c) and (d) are cross-section views of the multi-layer chip structure, with conductors shown in gray and insulators shown in black. (d) 1D slice of the potential showing the double well potential.

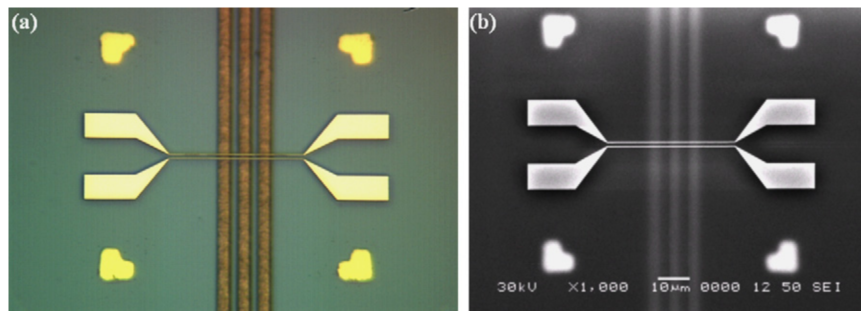

Fig. 5. Microscope (a) and SEM (b) images of a fabricated atom transistor chip (unreleased). Two horizontal copper wires above (width 300 nm, thickness 120 nm, length 40 μm). Three vertical copper wires below, embedded in the silicon substrate (width 3 μm and thickness 2 μm).

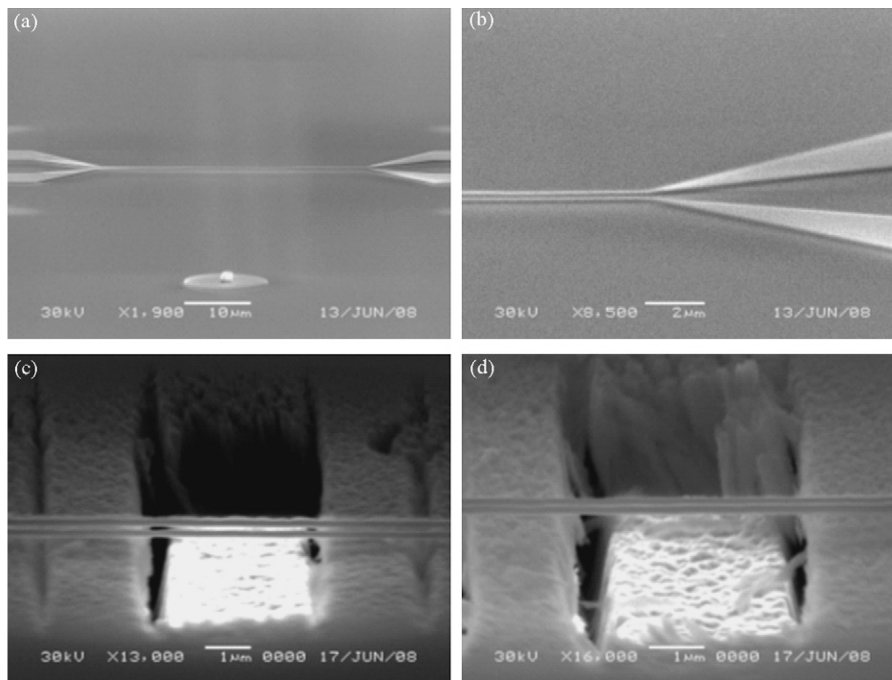

Fig. 6. SEM images of atom transistor chips during and after fabrication. (a) SEM image of the 300 nm wide copper wires on a planarized sputtered oxide surface. (b) A close-up SEM image of the electron-beam patterned copper wires (width: 300 nm, spacing between two wires: 1 μm). (c) SEM image of the suspended copper wires. The gap between the bridges and the bottom wire is 2 μm. (d) SEM image with different tilting angles of the released copper wires. The bridges are straight and the bottom copper wire is exposed after oxide window etch.

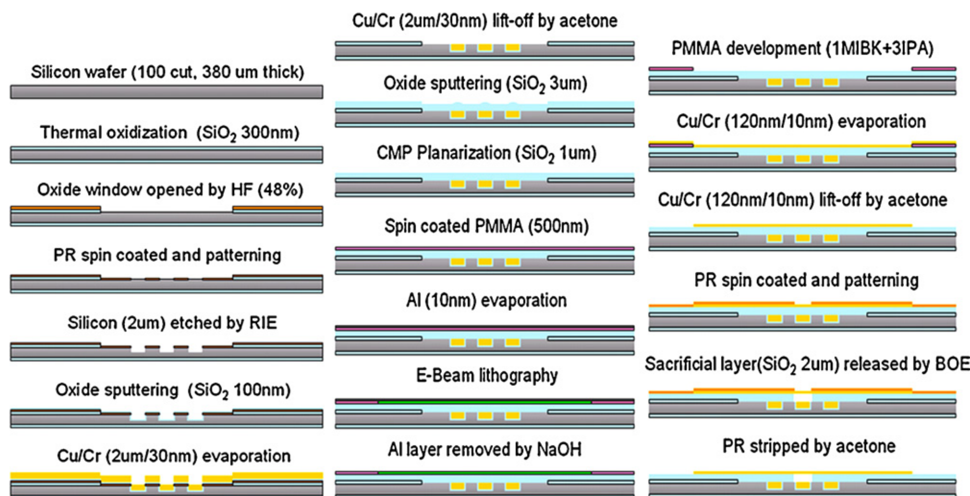

Fig. 7. Fabrication process for creating atom transistor chip.

raphy was 950 PMMA (polymethylmethacrylate) A7. It was spin coated on the oxide surface at 5000 rpm for 45 s. The thickness of the PMMA is around 500 nm. A 10 nm thick aluminum layer was then coated by thermal evaporation in order to provide an electrically conductive layer to avoid the charging effect in the SEM. The electron-beam patterning was performed with 30 kV acceleration voltage and 10 pA current. After electron-beam patterning, the aluminum layer was first removed by dipping in a diluted potassium hydroxide (NaOH) solution (100 ml of DI water with 10 drops of 50% concentration of NaOH) for 2 min. The PMMA layer was then developed in methyl iso-butyl ketone (MIBK) diluted with isopropanol (IPA) (MIBK:IPA = 1:3) and rinsed in pure IPA for 1 min each. The atom transistor chip wires were evaporated using an adhesion layer of chromium (5 nm) followed by copper (120 nm). The rest of the copper layer on the sputtered oxide was lifted off by acetone. The oxide release etch window was patterned by UV exposure with AZ 4620 photoresist. The copper nano-scale bridges were then released by buffered oxide etchant (BOE). After release, two copper nanowires were suspended above the bottom copper wires as shown in Fig. 6(c) and (d). Fig. 7 shows the overall fabrication process for creating atom transistor chips. After the atom transistor chip is made, it will be attached to a larger carrier chip, which in turn will be anodically bonded to a glass cell. This cell assembly is attached to an ultra-high-vacuum system and pumped down to a pressure of less than 10^{-10} Torr, which is low enough for the intended atomic physics experiments.

4. Characterization of the atom transistor chip

In order to observe tunneling rates under normal experimental conditions, we estimate that not more than 1–2 mA of current through each nanowire will be necessary. With the above described geometry, it possible to generate a double well trap with a trap separation of less than 1 μm and a barrier height of a few μK, as shown in Fig. 4(d). Designing for a safety factor of 5 we specify 10 mA as our maximum operating current. To verify that the fabricated nanowires would withstand the required currents we preformed a series of resistance and current capacity tests.

The resistances across the nanowires were measured by a four-point resistance measurement method at room temperature both in air and in a vacuum of 20 mTorr. The results are shown in Fig. 8. All of the measured resistances are randomly selected from 10 nanowires of each wire width. The copper nanowires with variable wire width (500 nm, 300 nm, and 200 nm) are all 120 nm thick. The average resistance values of the 500 nm, 300 nm and 200 nm wide

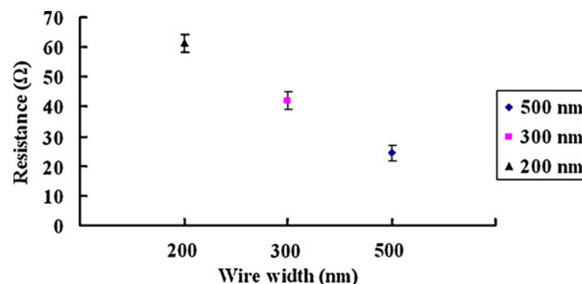

Fig. 8. Four-point resistances measurement performed on 10 wires of three different widths.

wires are 24 Ω, 42 Ω and 61 Ω, respectively. These values are about twice as large as those expected for bulk copper for the same geometry [23,24]. There is some variation in the size of the nanowires, which corresponds directly the resistance. This variation comes from imperfect control in the fabrication process, primarily from batch to batch changes in the copper deposition and the pattern development steps.

Several randomly selected nanowires with three different wire widths were connected to the bonding pads of the atom chip. Current, ranging from zero to several mA, was applied through the nanowires by a high resolution current power supply (HP 3245A Universal Source) until the wires burned out. The test results (Fig. 9) show that the burnout current of the released wires is several mA lower than the unreleased ones due to lack of thermal conduction through the oxide underneath the suspended wires. The burnout currents (tested in air) of the suspended 500 nm, 300 nm

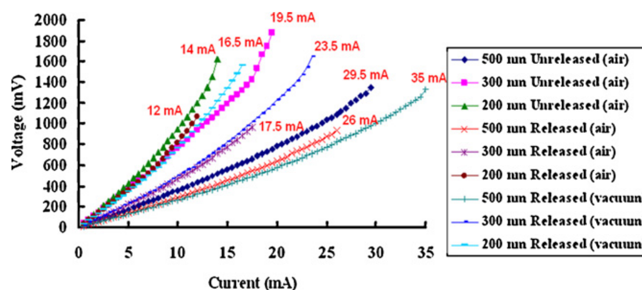

Fig. 9. Measured voltage as a function of applied current from three different wire widths (500 nm, 300 nm, and 200 nm) under different test conditions. “Air” means the test is performed at 1 atm and “vacuum” means the test is performed at 20 mTorr. The number at the end of each curve is the final burnout current.

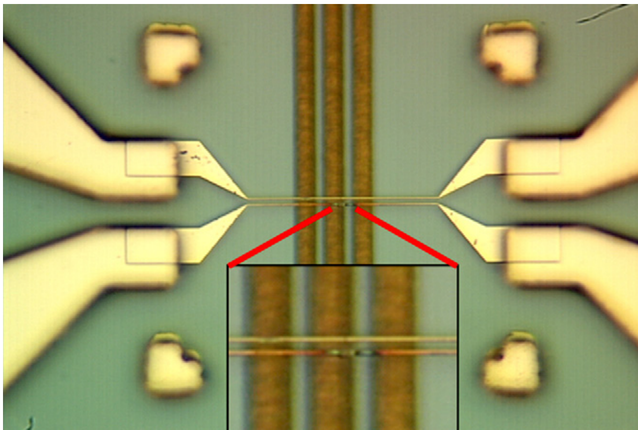

Fig. 10. Microscope image of a burned out suspended copper nanowire (300 nm wide, 120 nm thick, 40 μm long). Burned out current 12.5 mA.

and 200 nm wide wires are 26 mA, 17.5 mA and 12 mA, respectively. In addition, in order to better simulate the environment in which the wires are expected to perform several tests were performed under vacuum (20 mTorr). The results show that the burnout currents for each wire width were greater under vacuum than in air as shown in Fig. 9. This is due to a copper oxide layer forming on the wires when heated by current in air. Fig. 10 shows the microscope image of a burned out suspended copper nanowire (300 nm wide, 120 nm thick, 40 μm long). Burned out current is 12.5 mA. From the measured changes in resistances and the calculated current density, it is worth noting that under similar conditions all of the wires are able to carry roughly the same current density. In addition, the temperature of the wire can also be estimated by taking the resistance changes with temperature as $R = R_0[1 + \alpha(T - T_0)]$. Where R_0 is the resistance at a temperature of T_0 and α is the temperature coefficient of resistance. Under similar conditions, all wires burn out within about 10% of the same temperature as shown in Fig. 11. The measured changes in resistances as a function of current density are also shown in Fig. 12. Additionally, in order to mimic the situation in the actual atom transistor chip experiments, lifetime current tests were carried out in the vacuum (20 mTorr) with a pulse of 5 s and a relaxation time of 10 s, increasing the current by 1 mA for each pulse, until the nanowires burned out. The burnout currents of the 500 nm, 300 nm and 200 nm wide wires are 41 mA, 24 mA and 18 mA, respectively, corresponding to the current densities of 6.83×10^7 A/cm^2, 6.67×10^7 A/cm^2, and 7.5×10^7 A/cm^2. From our

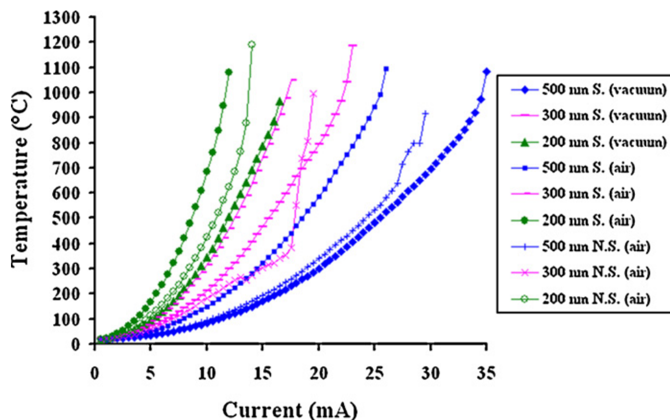

Fig. 11. Estimated burned out temperature of each wire. Under similar conditions all wires burn out within about 10% of the same temperature. “N.S.” and “S” refer to non-suspended wires and suspended wires. “Air” and “vacuum” refer to the test being performed at 1 atm and at 20 mTorr.

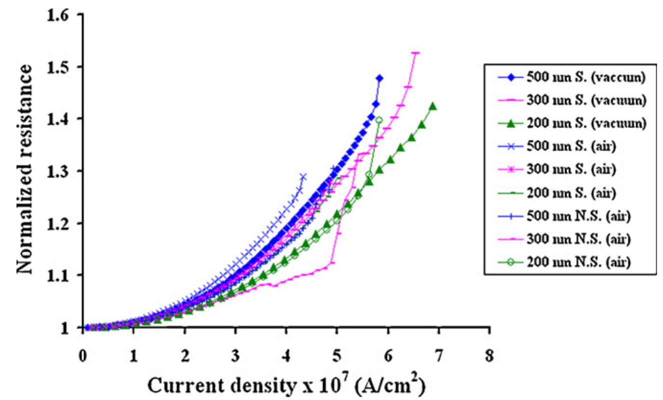

Fig. 12. Normalized resistance (R/R_0) as a function of current density from three different wire widths (500 nm, 300 nm, and 200 nm) under different test conditions. “N.S.” and “S” refer to non-suspended wires and suspended wires. “Air” and “vacuum” refer to the test being performed at 1 atm and at 20 mTorr.

electric current and lifetime test results, more than 10 mA of current can be successfully run through suspended copper nanowires for at least 5 s without burnout. Therefore, all of the tested wires were suitable for atom tunneling experiments.

5. Conclusions

To summarize, a fabrication process for the purpose of creating atom transistor chips for atom tunneling experiments has been developed. The fabrication combines the traditional UV-optical and electron-beam lithography in a double layer metallization process. Copper nanowires with wire widths ranging from 200 nm to 500 nm and suspended over a 10 μm wide and 2 μm deep trench, were successfully fabricated and tested in a low-pressure environment. The maximum current density of the 200 nm wide, 120 nm thick copper wires was measured at 7.5×10^7 A/cm^2, which is consistent with results reported by other groups [7], and sufficient for future tunneling experiments.

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Biographies

Ho-Chiao Chuang earned a B.S. in mechanical engineering at Da-Yeh University, Taiwan, in 2000 and a M.S. in the Department of Power Mechanical Engineering at National Tsing-Hua University, Taiwan, in 2002. He joined Professor Victor Bright's MEMS group in 2004 and earned his Ph.D. in 2008 from the Department of Mechanical Engineering at the University of Colorado at Boulder. During his graduate studies, he was also working in Professor Dana Anderson's group in the Department of Physics (JILA) at University of Colorado at Boulder. He is currently the Assistant Professor of Mechanical Engineering, National Taipei University of Technology, Taiwan, since 2009. His current research interests include tunable external cavity diode laser systems, fabrication of feedthrough atom trapping chips and atom transistor chips for atomic physics experiments, and micro/nanofabrication techniques.

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